We Claim:

1. An ESD protection circuit for a semiconductor integrated circuit (IC) having protected circuitry, comprising:

a multi-fingered NMOS transistor, each finger having a drain and source respectively coupled between an I/O pad of the IC and ground, and a gate of each finger for biasing said finger;

an ESD detector having a PMOS transistor comprising a source coupled to said I/O pad of the IC, and a gate coupled to a first supply voltage of the IC;

a parasitic capacitance formed between the supply line of the IC and ground; and

a transfer circuit having a first diode, where the cathode and anode are respectively coupled to the drain of the PMOS transistor and the gate of each finger of the NMOS transistor.

2. The ESD protection circuit of claim 1, wherein the gate of each finger of said NMOS transistor is coupled to a pre-driver during normal IC operation.

3. The ESD protection circuit of claim 1, wherein said multi-fingered NMOS transistor further comprises a plurality of active fingers and a plurality of ESD dummy fingers, wherein the gates of the active fingers are coupled to said first diode and a pre-driver.

4. The ESD protection circuit of claim 3, further comprising:

a first ground resistor coupled between said transfer circuit and ground.

5. The ESD protection circuit of claim 4, wherein said transfer circuit further comprises a second diode, where the cathode and anode of the second diode are respectively coupled to the drain of said PMOS transistor and the first ground resistor, said second diode further coupled to the gates of said ESD dummy fingers.

6. The ESD protection circuit of claim 5, further comprising a second ground resistor, coupled between the drain of said PMOS transistor and ground.

7. The ESD protection circuit of claim 6, further comprising:

a voltage limiter coupled between said transfer circuit and ground.

8. The ESD protection circuit of claim 7, wherein said voltage limiter comprises:

a first cascoded NMOS transistor having a source coupled to ground; and

a second cascoded NMOS transistor having the drain coupled to the gates of the plurality of active fingers, a gate coupled to a node formed between the drain of said PMOS transistor and the second ground resistor, and a source coupled to the drain and gate of the first cascoded NMOS transistor.

9. The ESD protection circuit of claim 6, further comprising a pre-driver control coupled to said pre-driver.

10. The ESD protection circuit of claim 9, wherein said pre-driver control comprises an NMOS transistor having a drain coupled to an input of said pre-driver, the source coupled to ground, and the gate coupled between said transfer circuit and the first ground resistor.

11. The ESD protection circuit of claim 10, wherein said pre-driver control further comprises a pull-up element coupled to a second supply line and the input of said pre-driver, where the second supply line has a voltage potential greater than a voltage potential at said input of said pre-driver.

12. The ESD protection circuit of claim 1, further comprising a PMOS transistor having a source and a N-well tie coupled to said first supply line and a drain coupled to the pad.

13. An ESD protection circuit for a semiconductor integrated circuit (IC) having protected circuitry, comprising:

a cascoded multi-fingered NMOS transistor, each finger having a first transistor and a second transistor, the drain of the first transistor and the source of the second transistor respectively coupled between an I/O pad of the IC and ground, the source of the first transistor coupled to the drain of the second transistor, and a gate of each transistor of each finger for biasing said finger;

an ESD detector having a PMOS transistor comprising a source coupled to said I/O pad of the IC, and an N-well tie coupled to the gate of the PMOS transistor;

a parasitic capacitance formed between the supply line of the IC and ground;

a transfer circuit comprising

a first diode having the anode and the cathode respectively coupled to the drain of the PMOS transistor and to the gate of the second transistor of each finger of the NMOS transistor; and

a second diode having the anode and the cathode respectively coupled to the drain of the PMOS transistor and the gate of the first transistor of each finger of the NMOS transistor; and

a plurality of serially coupled diodes coupled between a supply line and the gate of the PMOS transistor, where the cathodes and anodes of the serially coupled diodes respectively point towards the supply line and towards the gate of the PMOS transistor,

14. The ESD protection circuit of claim 13, wherein the gate of each second transistor of each finger is coupled to a pre-driver

15. The ESD protection circuit of claim 13, wherein said cascoded multi-fingered NMOS transistor further comprises a plurality of active fingers and a plurality of ESD dummy fingers, wherein the gates of the second transistor of the active fingers are coupled to said first diode and a pre-driver.

16. The ESD protection circuit of claim 13, further comprising:

a first ground resistor coupled between said transfer circuit and ground.

17. The ESD protection circuit of claim 16, wherein said transfer circuit comprises a third diode having an anode and cathode respectively coupled to the drain of said PMOS transistor and to the first ground resistor, said third diode having the cathode further coupled to the gates of the second transistors of said ESD dummy fingers.

18. The ESD protection circuit of claim 13, further comprising a second ground resistor, coupled between the drain of said PMOS transistor and ground.

19. The ESD protection circuit of claim 13, wherein said second diode is coupled to the gates of the first transistors of said active and ESD dummy fingers, said gates of the first transistors of said active and ESD dummy fingers further coupled to the supply line via a third resistor.

20. The ESD protection circuit of claim 19, further comprising:

a voltage limiter coupled between said transfer circuit and ground.

21. The ESD protection circuit of claim 20, wherein said voltage limiter comprises:

a first NMOS transistor having a source coupled to ground; and

a second NMOS transistor having the drain coupled to the gates of the second transistors of the plurality of said active and dummy fingers, a gate coupled to a node formed between the drain of said PMOS transistor and the second ground resistor, and a source coupled to the drain and gate of the first NMOS transistor;

a third NMOS transistor having the drain coupled to the gates of the first transistors of the plurality of active fingers, a gate coupled to the node, and a source coupled to the drain and gate of the first NMOS transistor;

a fourth NMOS transistor having the drain coupled to the gates of the second transistors of the plurality of ESD dummy fingers, a gate coupled to a node, and a source coupled to the drain and gate of the first NMOS transistor.

22. The ESD protection circuit of claim 20, further comprising a pre-driver control coupled to said pre-driver.

23. The ESD protection circuit of claim 22, wherein said pre-driver control comprises an NMOS transistor having a drain coupled to an input of said pre-driver, the source coupled to ground, and the gate coupled between said transfer circuit and the first ground resistor.

24. The ESD protection circuit of claim 13, further comprising a voltage-limiting resistor coupled between the gate and the N-well tie of the PMOS transistor, wherein said voltage-limiting resistor is further coupled to a well pump of said IC.

25. The ESD protection circuit of claim 13, further comprising an N-well pull-down loop, said N-well pull-down loop comprising:

a first NMOS transistor having a source coupled to ground and a gate coupled to the drain of the PMOS transistor and the second ground resistor; and

a second NMOS transistor having a source coupled to the drain of the first NMOS transistor, and a drain and a gate coupled to the N-well tie of the PMOS transistor.

26. The ESD protection circuit of claim 25, further comprising a breakdown device coupled to the N-well tie of said PMOS transistor and ground.

27. An ESD protection circuit for a semiconductor integrated circuit (IC) having protected circuitry, comprising:

a cascoded multi-fingered NMOS transistor, each finger having a first transistor and a second transistor, the drain of the first transistor and the source of the second transistor respectively coupled between an I/O pad of the IC and ground, the source of the first transistor connected to the drain of the second transistor, and a gate of each transistor of each finger for biasing said finger;

a PMOS transistor, having a source coupled to said I/O pad of the IC, and a gate coupled to an N-well tie;

a diode chain comprising a plurality of serially coupled diodes coupled between the supply line and the gate of the PMOS transistor, where the cathodes and anodes of the serially coupled diodes respectively point towards the supply line and towards the gate of the PMOS transistor;

a parasitic capacitance formed between the supply line of the IC and ground; and

at least one local substrate tie formed in proximity to the multi-finger NMOS transistor and coupled to the drain of the PMOS transistor.

28. The ESD protection circuit of claim 27, wherein said multi-fingered NMOS transistor further comprises a plurality of active fingers and a plurality of ESD dummy fingers, and a first resistor coupled to the drain of said PMOS transistor and ground, said at least one local substrate tie further coupled to the drain of said PMOS transistor and said first resistor.

29. The ESD protection circuit of claim 28, wherein the gates of the second cascoded transistor of the active fingers are coupled to a pre-driver, and the gates of the second cascoded transistor of said ESD dummy fingers are coupled to any one element comprising ground and at least one local substrate tie, and the gates of the first cascoded transistors of the active and ESD dummy fingers are coupled via a pull-up resistor to the supply voltage and further coupled via a first diode, wherein the cathode is coupled to said gates and the anode is coupled to the drain of said PMOS transistor and said first resistor.

30. An ESD protection circuit for a semiconductor integrated circuit (IC) having protected circuitry, comprising:

an SCR having at least one finger, each finger having a PNP transistor and an NPN transistor, where an emitter of the PNP and NPN transistors is respectively coupled between an I/O pad of the IC and ground, a base of the PNP transistor being coupled to a collector of the NPN transistor, and a base of the NPN transistor being coupled to a collector of the PNP transistor, and said NPN transistor of each finger further comprising a first gate for triggering said finger; and

a PMOS transistor, having a source and a drain respectively coupled to said I/O pad of the IC and the first gate of the NPN transistor, and a gate coupled to a supply voltage of the IC.

31. The ESD protection circuit of claim 30 further comprising:

a parasitic capacitance formed between the supply line of the IC and ground.

32. The ESD protection circuit of claim 30 further comprising:

a grounding resistor coupled between the first gate and ground.

33. The ESD protection circuit of claim 30 further comprising:

a parasitic capacitance formed between the supply line of the IC and ground; and

a grounding resistor coupled between the first gate and ground.

34. An ESD protection circuit for a semiconductor integrated circuit (IC) having protected circuitry, comprising:

a cascoded multi-fingered NMOS transistor, each finger having a first transistor and a second transistor, the drain of the first transistor and the source of the second transistor respectively coupled between an I/O pad of the IC and ground, the source of the first transistor coupled to the drain of the second transistor, and a gate of each transistor of each finger for biasing said finger;

an ESD detector having a PMOS transistor comprising a source coupled to said I/O pad of the IC, and a gate coupled to an N-well tie;

a transfer circuit comprising

a first diode having the anode and the cathode respectively coupled to the drain of the PMOS transistor and to the gate of the second transistor of each finger of the NMOS transistor; and

a second diode having the anode and the cathode respectively coupled to the drain of the PMOS transistor and the gate of the first transistor of each finger of the NMOS transistor; and

a breakdown device coupled to the N-well tie of said PMOS transistor, and ground.

35. The ESD protection circuit of claim 34, wherein the breakdown device consists of an element selected from a Zener diode, a regular junction diode, and a grounded gate NMOS device.